Please add the following new claim:

153 (New). An EL display comprising a display device according to claim 4.

REMARKS

Applicants will address each of the Examiner's objections and rejections in the order in which they appear in the Office Action.

Claim Objections

The Examiner has objections to Claims 68, 75 and 83 for informalities. Since Claims 68 and 75 are the same, Applicants are canceling Claim 75. Since there are two Claim 83, Applicants are canceling the second occurrence of Claim 83 and adding new Claim 153 (which includes the same subject matter as the second Claim 83). Therefore, it is respectfully submitted that these objections have been overcome.

Claim Rejections - 35 USC §112

The Examiner also rejects Claims 1-152 under 35 USC §112 as being indefinite. In particular, the Examiner objects to the phrases "conducted simultaneously" and "conducted next" in the independent claims.

Applicants have amended each of the independent claims herein to delete the objected to phrases. Therefore, it is respectfully submitted that the amended independent claims are not indefinite. Accordingly, it is requested that this objection now be withdrawn.

Claim Rejections - 35 USC §102

Applicants will address each of the Examiner's §102 rejections in the order in which they appear in the Office Action.

Rejection Over Okada

The Examiner also rejects Claims 1 and 11 under 35 U.S.C. §102(b) as being anticipated by Okada et al. This rejection is respectfully traversed.

Independent Claim 1 is directed to a display device. In order to provide a display device which enables multi-gray scale display without complicating the structure of D/A converter circuit, the display device of Claim 1 uses a voltage gray scale method, in which n bit information out of m bit digital video data inputted from an external is used, and a time ratio gray scale method in which (m-n) bit information is used. Further, a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period, as recited in amended Claim 1. This feature is shown, for example, in Fig. 8 and on page 15, lns. 12-14 of the specification.

Applicants respectfully submit that such a feature is not disclosed or suggested by Okada. Accordingly, independent Claim 1 and those claims dependent thereon are patentable over Okada. Therefore, it is requested that this rejection now be withdrawn.

Rejection Over Okumura

The Examiner rejects Claim 2 under 35 U.S.C. §102(b) as being anticipated by Okumura. This rejection is also traversed.

Independent Claim 2 is also directed to a display device and, as amended, also recites the feature of a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period.

Applicants respectfully submit that such a feature is not disclosed or suggested by Okumura. Further, Applicants disagree with the Examiner's assertion that D4 and D5 in Okumura are used for a time ratio gray scale method. Instead, Applicants submit that Okumura fails to teach the time ratio gray scale method because Okumura merely teaches that "D4 and D5 merely select any one of timing control signals A, B and C thereby the analog switch 106 is operated to turn OFF." Col. 6, lns. 23-25. Accordingly, independent Claim 2 and those claims dependent thereon are patentable over Okumura. Therefore, it is requested that this rejection now be withdrawn.

Hence, it is respectfully submitted that each of the §102 rejections have been overcome.

Claim Rejections - 35 U.S.C. §103

The Examiner also has the a number of rejections under 35 U.S.C. §103. Applicants will address each in the order in which they appear in the Office Action:

Rejection of Claims 3, 7, 34 and 38 Over Okada in view of Yasunishi.

The Examiner rejects Claims 3, 7, 34 and 38 under 35 USC §103 as being unpatentable over Okada in view of Yasunishi. This rejection is respectfully traversed.

Claim 3 recites that the display device comprises a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides the n bit digital video data to a source driver. The Office Action, however, fails to address where this feature is allegedly shown in the cited references.

Further, Claim 3 has been amended to recite that the circuit is formed over the same substrate as the active matrix circuit, the source driver and the gate driver. This feature is shown, for example, in Fig. 9 of the present application. Applicants do not believe that this feature is shown in either of the cited references. Independent Claim 7 is similarly not shown or suggested by the cited references.

Therefore, for at least the above-stated reasons, independent Claims 3 and 7 and those claims dependent thereon are patentable over the cited references, and it is requested that this rejection be withdrawn.

Rejection of Claim 4 Over Okumura in view of Yasunishi

The Examiner also rejects Claim 4 under 35 USC §103 as being unpatentable over Okumura in view of Yasunishi. This rejection is also respectfully traversed.

Claim 4 recites that the display device comprises a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides the n bit digital video data to a source driver. The Office Action, however, fails to address where this feature is allegedly shown in the cited references.

Further, Claim 4 has been amended to recite that the circuit is formed over the same substrate as the active matrix circuit, the source driver and the gate driver. This feature is shown, for example,

in Fig. 9 of the present application. Applicants do not believe that this feature is shown in either of the cited references.

Therefore, for at least the above-stated reasons, independent Claim 4 and those claims dependent thereon are patentable over the cited references, and it is requested that this rejection be withdrawn.

Rejection of Claims 5, 10 and 36 Over Okada

The Examiner further rejects Claims 5, 10 and 36 under 35 USC §103 as being unpatentable over Okada. This rejection is also respectfully traversed.

Independent Claim 5 is also directed to a display device and, as amended, also recites the feature of a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period.

As explained above, Applicants submit that such a feature is not disclosed or suggested by Okada.

Therefore, independent Claim 5 and those claims dependent thereon are patentable over the cited reference. Accordingly, it is requested that this rejection now be withdrawn.

Rejection of Claim 6 over Okumura in view of Okada.

The Examiner further rejects Claim 6 under 35 USC §103 as being unpatentable over Okumura in view of Okada. This rejection is also respectfully traversed.

Independent Claim 6 is also directed to a display device and, as amended, also recites the feature of a gray scale display level of one frame period corresponds to a value obtained by

averaging gray scale voltage levels inputted in each subframe period contained in said one frame period.

As explained above, Applicants respectfully submit that such a feature is not disclosed or suggested by Okada or Okumura.

Therefore, independent Claim 6 and those claims dependent thereon are patentable over the cited references. Accordingly, it is requested that this rejection now be withdrawn.

Rejection of Claim 8 over Okumura in view of Yasunishi and Okada.

The Examiner further rejects Claim 8 under 356 USC §103 as being unpatentable over Okumura in view of Yasunishi and Okada. This rejection is also respectfully traversed.

Claim 8 recites that the display device comprises a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides the n bit digital video data to a source driver. The Office Action, however, fails to address where this feature is allegedly shown in the cited references.

Further, Claim 8 has been amended to recite that the circuit is formed over the same substrate as the active matrix circuit, the source driver and the gate driver. This feature is shown, for example, in Fig. 9 of the present application. Applicants do not believe that this feature is shown in either of the cited references.

Therefore, for at least the above-stated reasons, independent Claim 8 and those claims dependent thereon are patentable over the cited references, and it is requested that this rejection be withdrawn.

Rejection of Dependent Claims

The Examiner also has the following rejections of the dependent claims:

1. Claims 12-17, 27, 29, 31, 41, 43, 45, 48, 50, 52, 55, 57, 59, 62, 64, 66, 69, 71, 73, 77, 79, 81, 89, 91, 93, 95, 97, 99, 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 127, 129, 131, 133, 135, 137, 139, 141, 143, 145, 147, 149 and 151 as being unpatentable over Yamazaki et al. or Holmes et al. or Kimura or Munyan or Stambolic et al. or Kleinschmidt et al. or Sato or Yun et al. in view of Okada et al. or of Okada et al. and Yasunishi.

2. Claims 26, 28, 30, 32, 33, 35, 37 and 39 as being unpatentable over Okumura or Okumura in view of Yasunishi or Okumura in view of Okada et al. or Okumura in view of Okada et al. and Yasunishi.

3. Claims 40, 42, 44, 46, 47, 49, 51, 53, 54, 56, 58, 60, 61, 63, 65, 67, 68, 70, 72, 74, 75, 76, 78, 80, 82, 90, 92, 96, 98, 100, 102, 104, 106, 108, 110, 112, 114, 116, 118, 120, 122, 124, 126, 128, 130, 132, 134, 136, 138, 140, 142, 144, 146, 150 and 152 as being unpatentable over Yamazaki et al. or Holmes et al. or Kimura or Munyan or Stambolic et al. or Kleinschmidt et al. or Sato or Yun et al. in view of Okumura or Okumura in view of Yasunishi or Okumura in view of Okada et al. or Okumura in view of Okada et al. and Yasunishi.

4. Claims 9, 20, 22 and 24 as being unpatentable over, in view of [*sic*] Okada et al. or Okada et al. and Yasunishi and further in view of Wu et al.

5. Claims 19, 21, 23 and 25 as being unpatentable over Okumura or Okumura in view of Yasunishi or Okumura in view of Okada et al. or Okumura in view of Okada et al. and Yasunishi and further in view of Wu et al.

6. Claims 18, 84, 85 and 87 as being unpatentable over Okada et al. or Okada et al. and Yasunishi and further in view of Bhargava.

7. Claims 83/2, 83/4, 86 and 88 as being unpatentable over Okumura or Okumura in view of Yasunishi or Okumura in view of Okada et al. or Okumura in view of Okada et al. and Yasunishi and further in view of Bhargava.

Each of these rejections is respectfully traversed as each of the dependent claims is allowable over the cited references for at least the reasons discussed above for the independent claims.

Accordingly, it is respectfully submitted that each of the rejections under 35 USC §103 have been overcome. Accordingly, it is requested that they now be withdrawn.

Conclusion

Therefore, it is respectfully submitted that the present application is now in a condition for allowance, and it is requested that it now be allowed.

If there is any further fee for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

_____

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Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

1.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix; and

a source driver and a gate driver which drive said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method, and (m-n) bit information is used for a time ratio gray scale method, where said m and said n are integers equal to or larger than 2 and satisfy m>n, and

[wherein said voltage gray scale method and said time ratio gray scale method are conducted simultaneously]

wherein a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period.

2.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix; and

a source driver and a gate driver which drive said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method, and (m-n) bit information is used for a time ratio gray scale method, where said m and said n are integers equal to or larger than 2 and satisfy m>n, [and

wherein said voltage gray scale method are conducted first and said time ratio gray scale method are conducted next]

wherein a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period, and

wherein said one frame period comprises 2^{m-n} subframe periods.

3.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix over a substrate;

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over said substrate, and

[wherein said voltage gray scale method and said time ratio gray scale method are conducted simultaneously, and]

wherein one frame image comprises 2^{m-n} subframes.

4.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix over a substrate;

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over said substrate, and

[wherein a voltage gray scale method are conducted first and a time ratio gray scale method are conducted next, and]

wherein one frame image comprises 2^{m-n} subframes.

5.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix; and

a source driver and a gate driver which drive said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method and (m-n) bit information is used for a time ratio gray scale method, where said m and said n are integers equal to or larger than 2 and satisfy m>n,

[wherein said voltage gray scale method and said time ratio gray scale method are conducted simultaneously, and]

wherein a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period, and

wherein an image is displayed by an image gray scale of $(2^m-(2^{m-n}-1))$ patterns.

6.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix; and

a source driver and a gate driver which drive said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method and (m-n) bit information is used for a time ratio gray scale method, where said m and said n are integers equal to or larger than 2 and satisfy m>n,

[wherein said voltage gray scale method are conducted first and said time ratio gray scale method are conducted next, and]

wherein a gray scale display level of one frame period corresponds to a value obtained by averaging gray scale voltage levels inputted in each subframe period contained in said one frame period,

wherein said one frame period comprises 2^{m-n} subframe periods, and

wherein an image is displayed by an image gray scale of $(2^m-(2^{m-n}-1))$ patterns.

7.(Amended) A display device comprising:

an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix over a substrate;

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, wherein said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over said substrate, and

[wherein a voltage gray scale method and a time ratio gray scale method are conducted simultaneously,